MT6169 RF System Datasheet

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Specifications are subject to change without notice.

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Document Revision History

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0.1	2013-07-21	YenHorng Chen	Initial draft
0.2	2013-07-22	Ryan Lee	Modified POD.
0.3	2013-10-14	Ryan Lee	Updated 3.2 CLK_SEL descriptions.
0.4	2013-11-19	Ryan Lee	Removed internal information.
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1.2	2014-03-12	Ryan Lee	1. Added table of content. 2. Added storage condition and package original pdf file in 3.1. 3. Added maximum power consumption and thermal resistance in 3.5.
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1.4	2014-05-05	YenHorng Chen	Modified RX NF.
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1.7	2015-05-28	YenHorng Chen	1. Add power/DCDC requirement 2. Add 2G IF and IQ loading description in section 7.

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1 Introduction

1.1 Overview

The MT6169 is a multi-mode multi-band transceiver in 40nm CMOS. The RF transceiver function is fully integrated. This document described the performance targets for the RF macro to be embedded in the overall product.

1.2 Key Features

- Full multi-mode RF solution (GGE/WCDMA/TDSCDMA/LTE)
    - *Multi-band LTE/WCDMA/TD-SCDMA/Quad-band GGE*
    - *16QAM UL/64QAM DL (HSPA+/LTE)*
    - *2G/3G/4G co-banding*
    - *RxD support (8 RxD ports)*

- Direct Conversion (LTE/3G), Two Point Modulation (TPM) for GMSK and Small Signal Polar for 8-PSK
    - Dedicated power detection circuits for power control over specific power range
- Hybrid Direct-Conversion (4G/3G) / Low-IF (GGE, DC-HSDPA) receiver
- Low supply current & operation directly from DC-DC converter
- 26MHz internal DCXO or external VCTCXO operation (with integrated AFC DAC)
    - Three low noise additional Clock Drivers for clocking connectivity / peripheral IC's
    - Ultra Low power 32KHz mode
- Support RF Calibration features for key Rx and Tx specifications (Image rejection, LO feedthrough, DC offset)
- Temperature Measurement sub-system

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2 Block Diagram and Application Diagram

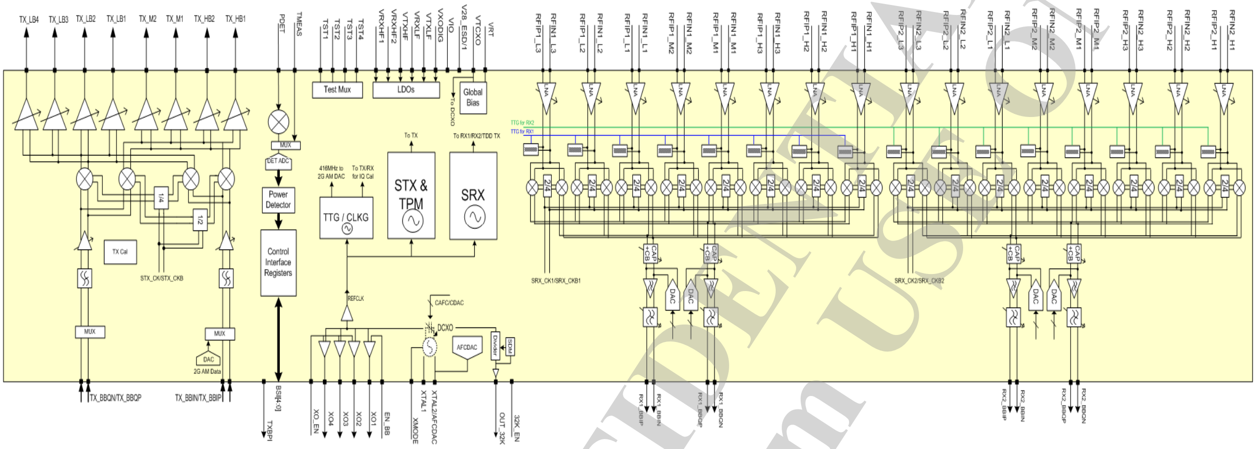

Figure 2-1. RFSYS block diagram

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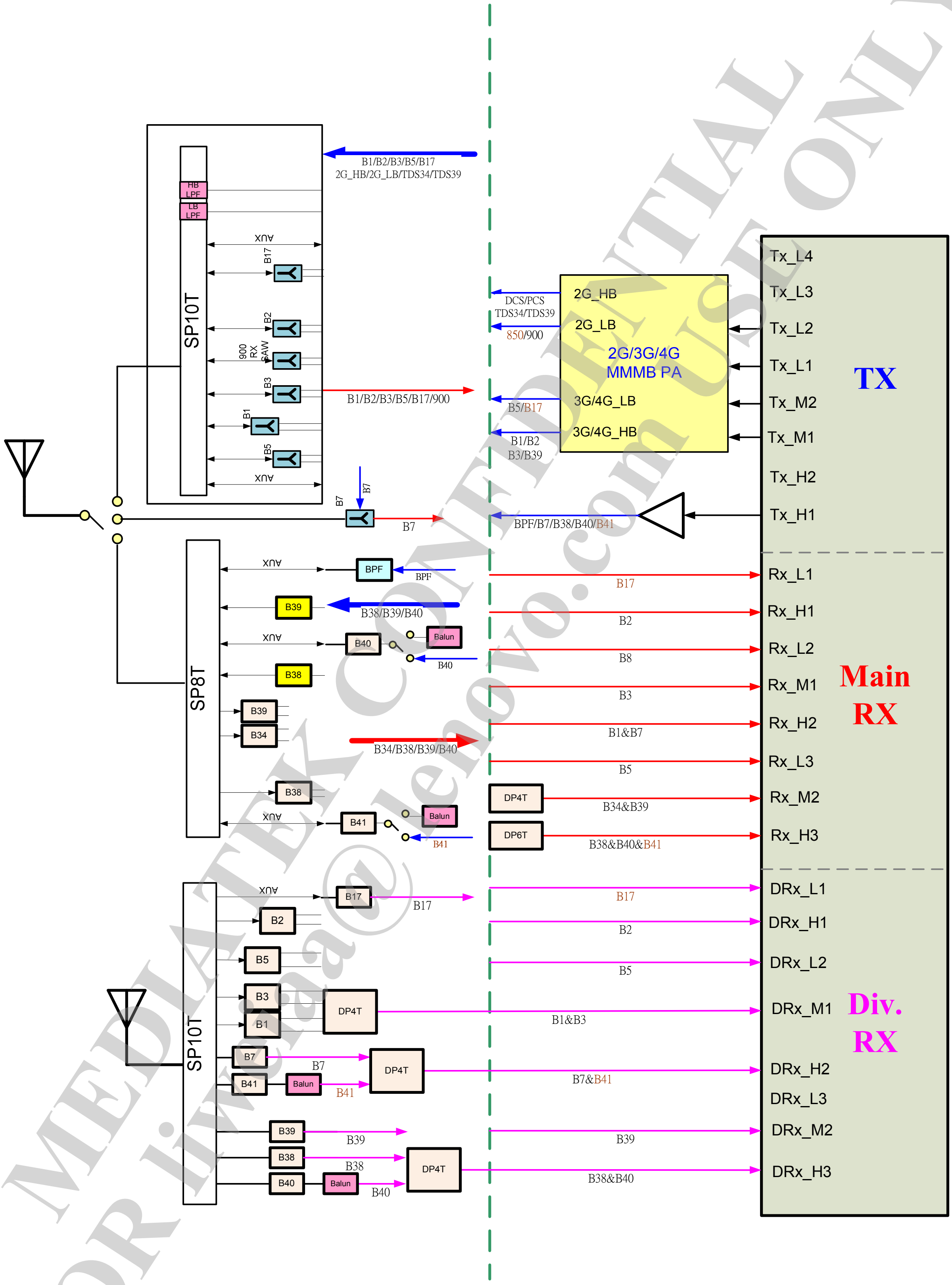

Figure 2-2. Applications diagram

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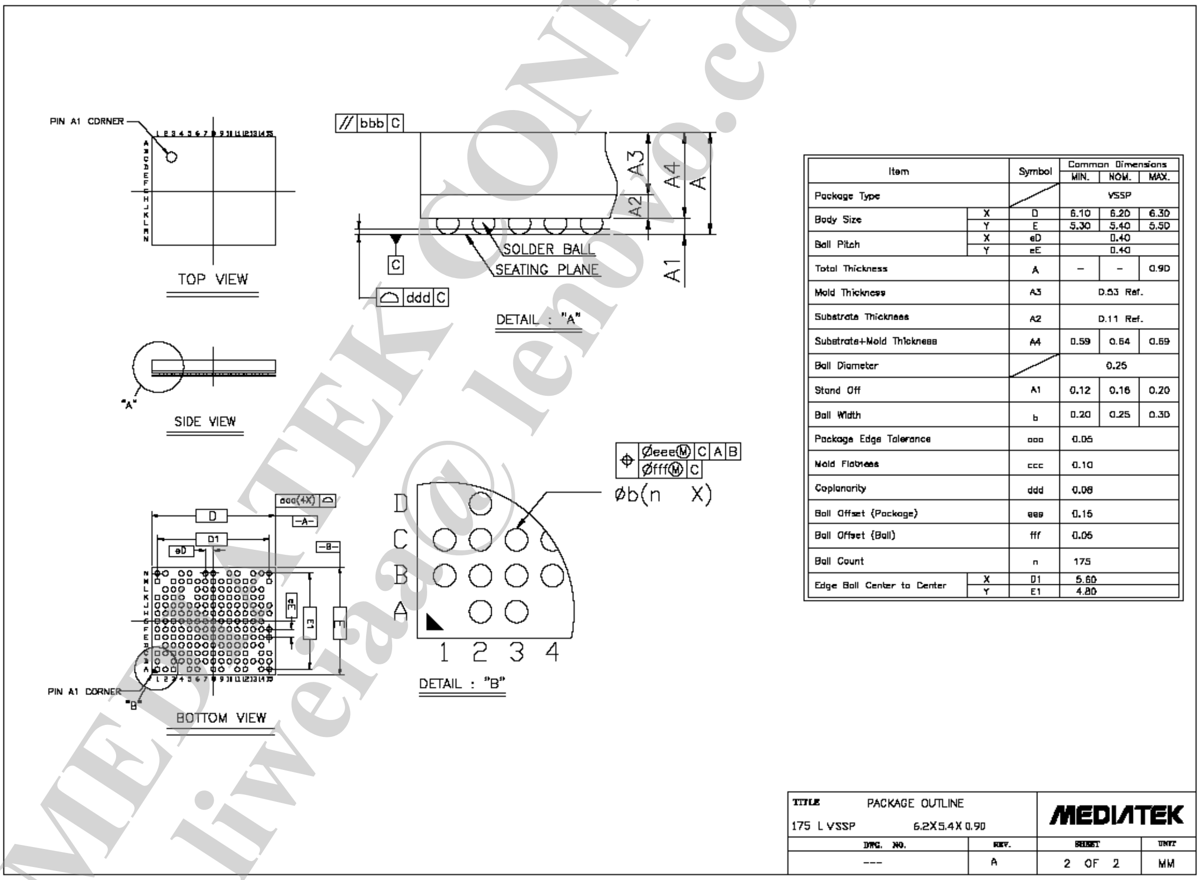
3 General Specifications

3.1 Packaging

Wirebond aS3 is currently considered for this product.

Parameter	Single die
Body Size	6.2x5.4mm
Ball Spacing	0.4mm
Ball number	175
Storage Condition (temperature <40 degree, relative humidity<90%)	12 months



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			VSSP		
Body Size	X	D	6.10	6.20	6.30
	Y	E	5.30	5.40	5.50
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Total Thickness		A	–	–	0.90
Mold Thickness		A3	0.53 Ref.		
Substrate Thickness		A2	0.11 Ref.		
Substrate+Mold Thickness		A4	0.59	0.64	0.69
Ball Diameter			0.25		
Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	175		
Edge Ball Center to Center	X	D1	5.60		
	Y	E1	4.80		

MT6169 POD.pdf

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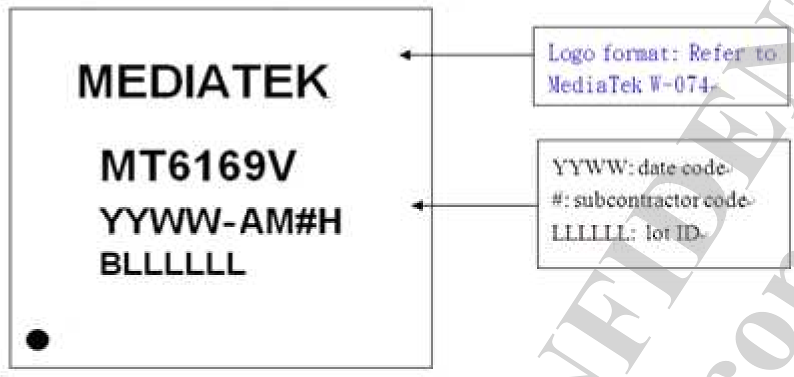
3.2 Ordering Information

Order#	Marking	Temp.range	Package
MT6169V/A	MT6169V	-20C~60C	VSSP

3.3 IC Marking



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F I/O List

Category	Pin Name				Description
	Name	Default	I/O	GPIO/RF Pin	
RF I/O	RX1P_H1		I	RF	RX1 HB1 input
	RX1N_H1		I	RF	RX1 HB1 input
	RX1P_H2		I	RF	RX1 HB2 input
	RX1N_H2		I	RF	RX1 HB2 input
	RX1P_H3		I	RF	RX1 HB3 input
	RX1N_H3		I	RF	RX1 HB3 input
	RX1P_M1		I	RF	RX1 MB1 input
	RX1N_M1		I	RF	RX1 MB1 input
	RX1P_M2		I	RF	RX1 MB2 input
	RX1N_M2		I	RF	RX1 MB2 input
	RX1P_L1		I	RF	RX1 LB1 input
	RX1N_L1		I	RF	RX1 LB1 input
	RX1P_L2		I	RF	RX1 LB2 input
	RX1N_L2		I	RF	RX1 LB2 input
	RX1P_L3		I	RF	RX1 LB3 input
	RX1N_L3		I	RF	RX1 LB3 input
	RX2P_H1		I	RF	RX2 HB1 input
	RX2N_H1		I	RF	RX2 HB1 input
	RX2P_H2		I	RF	RX2 HB2 input
	RX2N_H2		I	RF	RX2 HB2 input
	RX2P_H3		I	RF	RX2 HB3 input
	RX2N_H3		I	RF	RX2 HB3 input
	RX2P_M1		I	RF	RX2 MB1 input
	RX2N_M1		I	RF	RX2 MB1 input
	RX2P_M2		I	RF	RX2 MB2 input
	RX2N_M2		I	RF	RX2 MB2 input
	RX2P_L1		I	RF	RX2 LB1 input
	RX2N_L1		I	RF	RX2 LB1 input
	RX2P_L2		I	RF	RX2 LB2 input
	RX2N_L2		I	RF	RX2 LB2 input
	RX2P_L3		I	RF	RX2 LB3 input
	RX2N_L3		I	RF	RX2 LB3 input
	TX_H1		O	RF	TX HB1 output
	TX_H2		O	RF	TX HB2 output
	TX_M1		O	RF	TX MB1 output
	TX_M2		O	RF	TX MB2 output
	TX_L1		O	RF	TX LB1 output
	TX_L2		O	RF	TX LB2 output
	TX_L3		O	RF	TX LB3 output
	TX_L4		O	RF	TX LB4 output
	TX_DET		I	RF	TX detection path input
BB I/O	RX1_BBIP		O	BB	RX1 BB I output
	RX1_BBIN		O	BB	RX1 BB I output
	RX1_BBQN		O	BB	RX1 BB Q output
	RX1_BBQP		O	BB	RX1 BB Q output

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Category	Pin Name				Description
	Name	Default	I/O	GPIO/RF Pin	
	RX2_BBIP		O	BB	RX2 BB I output
	RX2_BBIN		O	BB	RX2 BB I output
	RX2_BBQN		O	BB	RX2 BB Q output
	RX2_BBQP		O	BB	RX2 BB Q output
	TX_BBIP		I	BB	TX BB I input
	TX_BBIN		I	BB	TX BB I input
	TX_BBQN		I	BB	TX BB Q input
	TX_BBQP		I	BB	TX BB Q input
BSI Interface	BSI_EN		I	GPIO	BSI enable
	BSI_CLK		I	GPIO	BSI clock
	BSI_DATA0		I/O	GPIO	BSI input/output data
	BSI_DATA1		I/O	GPIO	BSI input/output data
	BSI_DATA2		I/O	GPIO	BSI input/output data
TCVCXO/ DCXO	XTAL1		I	RF	XO input
	XTAL2/ AFCDAC		I/O	RF	XO input/ AFCDAC output
	XO1		O	RF	DCXO buffer 1 output for ABB/DBB
	XO2		O	RF	DCXO buffer 2 output for
	XO3		O	RF	DCXO buffer 3 output
	XO4		O	RF	DCXO buffer 4 output
	OUT_32K		O	RF	32k output
	CLK_SEL	0	I		DCXO buffer 2, 3, 4 enable
	EN_BB		I		Global static enable
	DCXO_32KEN	0	I		32k enable
	XMODE	0	I		Select DCXO (1) or TCVCXO (0)
Test Ports	TST1		O	RF	Test pin 1
	TST2		O	RF	Test pin 2
	TST3		O	RF	Test pin 3
	TST4		O	RF	Test pin 4
	TXBPI		O	RF	TX DCOC feedback to BB
	TMEAS		I	DC	Temperature measurement
	VRT		O	RF	External resistor pin
Voltage Supply	VRXHF1		VDD	RF	DCDC 1.8V supply for RX1
	VRXHF2		VDD	RF	DCDC 1.8V supply for RX2
	VRXLF		VDD	RF	DCDC 1.8V supply for RX PLL (exclude RX VCO) and RXDYN
	VTXHF		VDD	RF	DCDC 1.8V for TX
	VTXLF		VDD	RF	DCDC 1.8V supply for TX detection path IF part, TX PLL (exclude TX VCO) and TXDYN
	VIO18		VDD	RF	Always on 1.8V
	VXO_DIG		VDD	RF	Always on power for GS and DCXO DIG
	VTCXO28		VDD	RF	2.8V for DCXO/TCVCXO
	V28ESD		VDD	RF	2.8V just for ESD power.
	TXO_GND		GND	RF	TX output ground

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Category	Pin Name				Description
	Name	Default	I/O	GPIO/RF Pin	
	TXDET_GND		GND	RF	TX DET ground

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3.4 Ball Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	RFIP2_LB3	RFIN2_MB1	RFIP2_MB1		RFIP2_LB2	RFIN2_HB1		RFIN1_HB3	RFIP1_HB3		RFIP1_LB3	RFIN1_HB2		RFIN1_LB2	RFIP1_LB2
B	RFIN2_LB3		RFIN2_HB2	RFIP2_HB2	RFIN2_LB2	RFIP2_HB1	RFIN2_LB1	RFIP2_LB1	RFIN1_MB2	RFIP1_MB2	RFIN1_LB3	RFIP1_HB2	RFIN1_MB1	RFIP1_MB1	RFIN1_HB1
C	RFIP2_MB2	RFIN2_MB2	GND	GND	GND	GND	GND	VRXHF2	GND	GND	GND	GND		RFIN1_LB1	RFIP1_HB1
D		RFIP2_HB3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VRXHF1	RFIP1_LB1	
E	GND	RFIN2_HB3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TXO_GND	TXO_GND	TXO_GND
F	OUT_32K	GND	TST1	GND	GND	GND	GND	GND	GND	GND	GND	GND	TXO_GND	TX_HB2	TX_HB1
G	XO3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TXO_GND	TX_MB1	
H	XO2	XO4	GND	GND	GND	GND	GND	GND	GND	GND	GND	TST4	TXO_GND	TX_MB2	TX_LB4
J	VTCXO	32K_EN	GND	GND	BSI_D1	BSI_D0	BSI_EN	GND	GND	GND	GND	GND	TXO_GND	TX_LB2	TX_LB3
K	XTAL2	XTAL1	GND	BSI_D2		BSI_CK	GND	GND	GND	TXBPI	VTXLF	GND	TXO_GND	TX_LB1	
L		XMODE	GND	VDCXO_DIG		GND	GND	GND	GND	GND	GND	GND	DET_GND	TXO_GND	
M	XO1		VIO	RX2_BBQP	RX2_BBIP	RX1_BBQP	RX1_BBQN	VRXLF	TMEAS	TST2	V28_ESD1	TST3	TXDET		TX_BBIP
N	CLK_SEL	EN_26M_BB		RX2_BBQN	RX2_BBIN		RX1_BBIN	RX1_BBIP		VRT	VTXHF		TX_BBQP	TX_BBQN	TX_BBIN

Figure 3-1. Ball map

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3.5 Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.	Unit	Notes
Supply VTCXO28		-0.3	3.3	V	
Supply VIO18		-0.3	2.0	V	
Supply VXODIG		[-]	[-]	V	1. Connects to VIO18 in normal case 2. Connects to VTCXO28 in 32K-less case 3. In ATPG mode, it connects to an independent supply with 1.4-V maximum voltage
Supply VRF18		-0.3	2.0	V	
Maximum Power Consumption			0.55	W	
Junction Temperature			125	°C	
Thermal Resistance	Θja (c/w)		60	(c/w)	
	Θjc (c/w)		25.2	(c/w)	
ESD Protection	HBM – analog and digital I/O	±2000		V	
	HBM – RF I/O	±2000		V	PDET, Rx inputs, Tx outputs
	FICDM – analog and digital I/O	±250		V	target - no current corporate requirement
	FICDM– RF I/O	±250		V	PDET, Rx inputs, Tx outputs target - no current corporate requirement
	MM – analog and digital I/O	±200		V	
	MM – RF I/O	±100		V	PDET, Rx inputs, Tx outputs

Notes

1. No DC input should be directly applied to the Rx inputs. Matching network should either be a series capacitor/inductor or shunt inductor (RXn/RXnB)
2. Tx Output: no DC should be applied under any circumstances (AC coupling required for those PA's with DC at the input)

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3.6 Operating Conditions

Within the operating range the IC operates as per the functional description.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Operating temperature		-20		60	degree
Supply VIO18		1.7	1.8	1.9	V
SMPS Supply VRF18		1.75	1.825	1.9	V
Linear Supply VTCXO28		2.7	2.8	2.9	V
Supply VXODIG	Normal function mode	Connects to VIO18			
Supply VXODIG	32K-less mode	Connects to VTCXO28			
Supply VXODIG	ATPG mode – LDO's bypassed in this mode	1.1	1.2	1.4	V
Receiver Front End					
RX input frequency range	See Receiver Section for detailed frequency ranges				
Rx required amplitude balance	All Rx input pairs	-1		+1	dB
Rx required phase balance	All Rx input pairs	-10		+10	deg
Transmitter					
Tx Frequency Range	See Transmitter Section for detailed frequency ranges				
Tx O/P VSWR	All Phases ZL = 50Ω			2:1	
Clock Buffers					
XO1, XO2, XO3, XO4 Load (Rload||Cload) to GND	Cload	See section [7.3]			pF
	Rload				kΩ
Reference Clock Input (VCTCXO)					
Reference Clock Frequency			26.0		MHz
Reference Clock Input Voltage Swing	AC coupled at input pin	700		1500	mVpp
Duty Cycle		40		60	%
Phase Noise – note 2	@ F_{offset} = 100Hz		<-103	-100	dBc/Hz
	@ F_{offset} = 1KHz		<-133	-130	dBc/Hz
	@ F_{offset} = 10KHz		<-147	-144	dBc/Hz
	@ F_{offset} = 100KHz		<-149	-146	dBc/Hz
Harmonic Content	HD2 @ 52MHz			-8	dBc
	HD3 @ 78MHz			-10	dBc
	HD4 @ 104MHz			-20	dBc
Start-up time	|Δf|<1ppm to >90% of final amplitude			3	ms
Crystal Requirements					
2 Crystal types are supported (Crystal #1 3225 body size / Crystal #2 2520 body size)					

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Parameter	Conditions	Min.	Nom.	Max.	Unit
Nominal Load Capacitance	Crystal #1		7.5		pF
	Crystal #2		7.0		pF
Initial Frequency error				±10	Ppm
ESR				30	Ω
Drive level				100	µW
Pullability	Crystal #1	-10%	32	+10%	ppm/pF
	Crystal #2	-10%	27	+10%	ppm/pF

Note 1

The supportable ambient temperature range will depend on the thermal impedance of the package used and the exact operational state as well as the end application thermal design (housing, PCB etc).

Junction temperature is a more reliable indication of the actual operational range.

Note 2

The input clock requirement specified is defined to meet receiver and transmitter phase noise requirements e.g. IC EVM specification. Certain connectivity requirements may require better specifications than this. See clock buffer in section [7]. The clock source (non DCXO mode) can either be an external VCTCXO/VCXO module or alternatively another transceiver clock buffer when considering multiple transceiver applications.

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4 Supply Specification

4.1 External Power Supplies and Interfaces

The RFSYS macro operates from four power supplies.

Supply Name	Usage	Regulator Type	Output Voltage
VTCXO28	Regulated supply for VCTCXO/DCXO	Linear	2.8V
VRF18	Regulated supply for all major sub-systems	Switching	1.825V
VIO18	Always-on supply for interface and register retention	Switching	1.8V
*VXODIG	Connects to VIO18 in normal mode and VTCXO28 in 32K-less mode	Linear or Switching	1.8V / 2.8V

* Since VXODIG is connected to VIO18 or VTCXO28, its current is merged to VIO18 or VTCXO28 in this section

Supply	Regulator Type	Vtyp [V]	Tolerance [mV]	Special Request
VIO[1.8V] / VXO_DIG [1.8V]	Linear or Switching	1.80	±100mV	very low quiescent current as always on
VTCXO [2.8V]	Linear	2.80	±100mV	low noise for use on DCXO/VCTCXO, must have very low quiescent current for 32KHz elimination mode
VRF[1.8V]	Switching	1.825	±75mV	maximum ripple = 20mVpk-pk default switching frequency 2.0MHz +/- 5% (PWM) for on-chip oscillator / lock to 26MHz preferred

Below is the total battery current measured when the chip is operating in the mode described using the recommended register settings. For ease of comparison and benchmarking it is assumed no peripheral clock buffers are enabled (except 26MHz co-clock case in the deep sleep mode).

Mode	Conditions	I_{VIO18}		I_{VTCXO}		I_{VRF18}		I_{BAT}		Unit
		Nom	Max	Nom	Max	Nom	Max	Nom	Max	
Deep Sleep (normal)	VIO18 only present, no other supplies, no 26MHz clock request	10	16	0	0	0	0			µA
Deep Sleep (32K-less)	DCXO enabled in the 32KHz low power mode	0	0	130		0	0			µA
Standby	DCXO and Global Static have Power. VRF18 not present	0.12	0.23	4		0	0			mA
Sleep	All power present (VIO18, VTCXO28, VRF18) but Rx / Tx not enabled	0.12	0.23	4		4				mA
RX ON	20MHz / no Rx-D / LNA high gain (B1/B7/B20)	0.12	0.23	4		74/77/63				mA
	20MHz / no Rx-D / LNA high gain (B38/B39/B40)	0.12	0.23	4		82/78/81				mA

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Mode	Conditions	I_{VIO18}		I_{VTCXO}		I_{VRF18}		I_{BAT}		Unit
		Nom	Max	Nom	Max	Nom	Max	Nom	Max	
	20MHz / no Rx-D / LNA mid gain (B1/B7/ B20)	0.12	0.23	4		64/67/ 56				mA
	20MHz / no Rx-D / LNA mid gain (B38/B39/B40)	0.12	0.23	4		73/68/ 72				mA
	20MHz / Rx-D / LNA high gain (B1/B7/B20)	0.12	0.23	4		123/127 /106				mA
	20MHz / Rx-D / LNA high gain (B38/B39/B40)	0.12	0.23	4		132/121 /129				mA
	20MHz / Rx-D / LNA mid gain (B1/B7/B20)	0.12	0.23	4		103/107 /93				mA
	20MHz / Rx-D / LNA mid gain (B38/B39/B40)	0.12	0.23	4		113/96/ 110				mA
	WCDMA/GSM/EDGE/TDSCDMA/ LNA high gain (HB/LB/TDSCDMA)	0.12	0.23	4		67/62/ 71				mA
	WCDMA/GSM/EDGE/TDSCDMA/ LNA mid gain (HB/LB/TDSCDMA)	0.12	0.23	4		59/55/ 63				mA
	Pout=Pmax (B7/B1/B13/B20)	0.12	0.23	4		196/177 /160/15 7				mA
TX ON	Pout=Pmax-12dB (B7/B1/B13/B20)	0.12	0.23	4		116/110 / 100/97				mA
	GMSK Mode (HB/LB)	0.12	0.23	4		76/72				mA
	8-PSK Mode Pout=Pmax (HB/LB)	0.12	0.23	4		140/148				mA
	8-PSK Mode Pout=Pmax-12dB(HB/LB)	0.12	0.23	4		74/81				mA

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5 Reference Clock Specification

MT6169 RF system integrates a core 26MHz XTAL oscillator (DCXO), AFCDAC and a 32KHz low power mode. Also all the clock buffers external and internal are integrated in this system.

The mode of operation (internal DCXO or external VCTCXO) is selected via the input XMODE from the baseband with the following function

XMODE	Mode
LOW	External CLK (VCTCXO)
HIGH	DCXO

In Crystal mode the XTAL is connected directly between XO1 and XO2.

In VCTCXO mode XO2 pin is reconfigured to be the AFCDAC output and XO1 the VCTCXO clock input pin.

Since the state of XMODE is latched into the module then the baseband configuration can take place using a pin state “trapping” scheme on power up if desired.

5.1 DCXO Specification

Parameter	Test condition	title	Unit	Min	Nom	Max
Supply current in sleep (Core+one buffer for baseband)	VCTCXO=2.8V; output differential current $75uA_{single,p-p}$ to BB	$I_{dcxo,sleep}$	mA		2	
Supply current in TRX (Core+ buffers for baseband, 3-wire, SX)	VCTCXO=2.8V; output differential current $75uA_{single,p-p}$ to BB	$I_{dcxo,trx}$	mA			3
Supply current for other systems (each extra buffer)	VCTCXO=2.8V; loading refer to Table3	$I_{dcxo,buf}$	mA			1.5
Leakage current	ENdcxo(hardware) = 0V	$I_{leakage}$	uA			1
Center operating frequency	Internal resonant; crystal definition in Section [3.6]	F_{dcxo}	MHz		26	
Duty cycle	Square wave in high driving mode		%	45	50	55
Static range	CapID coding 0 ~ 255 at middle AFC coding. Nominal crystal TS definition in Section [3.6]	R_{static}	ppm		±50	
	At middle CAFC code.		ppm	17		

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	Minimum crystal TS definition in Section [3.6]. Smallest amount of negative range from 26MHz as -15% capacitor corner.					
	At mid CAFC code. Minimum crystal TS definition in Section [3.6]. Smallest amount of negative range from 26MHz		ppm	32		
	At middle CAFC coding. Minimum crystal TS definition in Section [3.6]. Smallest amount of positive range from 26MHz as +15% capacitor corner		ppm	17		
	At mid CAFC code. Minimum crystal TS definition in Section [3.6]. Smallest amount of positive range from 26MHz		ppm	32		
CapID bits	CDAC		bit		8	
Dynamic range	CAFC coding 0 ~ 8191 at mid CapID. Nominal crystal TS definition in Section [3.6].	$R_{dynamic}$	ppm		±30	
	Mid CAFC code and tune CapID to target frequency if FL has ±10ppm error. Minimum crystal TS definition in Section [3.6]. As -15% capacitor corner		ppm	±15		
	Mid CAFC code and tune CapID to target frequency if FL has ±10ppm error. Minimum crystal TS definition in Section [3.6].		+-ppm	18		
CAFC bits			bit		13	
CAFC tuning step	Average AFC frequency step , for the CAPID that is closest to 26MHz		ppm		0.007	
CAFC tuning step frequency linearity	No need Linearity Calibration to save time. Cafc at middle and tune CapID to target frequency if FL has +-10ppm error.		%		50	60
CAFC tuning step spike	for all adjacent CAFC coding, especially as capacitor array changes rows or columns	D	LSB	0		1 AFC LSB range
CAFC Slope Curve	CAFC coding 0 ~ 8191 for all CapID				smooth and Monoto	

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					nic	
CAFC settling time	CAFC coding changes 2000 at one time. Delta f < 1ppm.	T_{settle}	us		150	200
Crystal input pins	Specific foundries		pin		2	
Crystal size					Both 2520& 3225	

5.2 Reference Input Buffer Specification (XO1/REFIN)

The input conditions are given in section [3.5].

Parameter	Conditions	Min	Nom	Max	Unit
Input Impedance – Rp	Rp || Cp @ 26MHz	0.8	1		kΩ
Input Impedance – Cp	Rp || Cp @ 26MHz		10	12	pF

This pin should be AC coupled when used with an external clock source.

5.3 Reference Output Buffer(s) Specification

There are 3 reference clock output buffers driving out from the chip. They can be used as reference clock for other chips and application.

External DC block is assumed on all buffer outputs. All buffers are identical designs.

Parameter	Conditions	Min	Nom	Max	Unit
Buffer output Swing	Square wave @ Zload= Cp || Rp	700		1200	mVp-p
Zload (Rp||Cp)	Rp	3			kΩ
	Cp			30	pF
Duty Cycle		40		60	%
Rise/Fall Time	10% to 90% of signal swing @ Cload=30pF [normal drive mode]			6.5	ns
SSB phase noise	1Hz offset [30pF load, normal drive mode]			-50	dBc/Hz
	5Hz offset [30pF load, normal drive mode]			-73	dBc/Hz
	10Hz offset [30pF load, normal drive mode]			-80	dBc/Hz
	100Hz offset [30pF load, normal drive mode]			-105	dBc/Hz
	1kHz offset [30pF load, normal drive mode]			-131	dBc/Hz
	10kHz offset [30pF load, normal drive mode]			-145	dBc/Hz

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Parameter	Conditions	Min	Nom	Max	Unit
	100KHz offset [30pF load, normal drive mode]			-150	dBc/Hz
Current Consumption	Zload = 20pF (each buffer)		1.0		mA

5.4 32kHz Mode

In low power mode a 32kHz clock is produced by using a fractional-N divider (1st order Sigma Delta Modulated) to replace the normal 32kHz XTAL (watchdog). In this mode the CDAC and CAFC capacitance is minimized so that the XTAL core can operate from a significantly reduced bias current).

Parameter	Conditions	Min	Nom	Max	Unit
Frequency			32768		Hz
DCXO Current Consumption	Low Power Mode With all capacitors switched off and auto-amplitude calibration is on		~200		µA
Duty Cycle				80	%
Settling Time				3	ms
Frequency variation	After system calibration			±2	ppm
	Over temperature -25degC to 75degC			15	ppm
	Uncalibrated – total variation			200	ppm

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6 Transmitter

All transmitter characteristics are listed in this section. Typical specifications are for mid-band channel frequency, and under typical operating conditions. Min/Max specifications are for extreme operating voltage and temperature conditions.

6.1 Tx Block Diagram

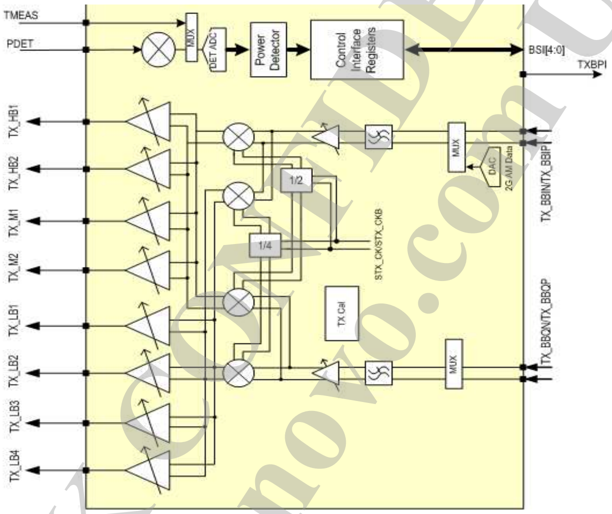

Figure 6-1. Tx block diagram

TXO	Band supported
H1, H2	1, 2, 3, 4, 7, 9, 10, 23, 25, 33, 34, 38, 39, 40, 41
M1, M2	1, 2, 3, 4, 9, 10, 11, 21, 23, 24, 25, 33, 34, 39
L1 – L4	5,, 6, 8, 12, 13, 14, 17, 18, 19, 20, 26, 27, 28
M1, M2, L3, L4	2G

TXO	Min Freq (MHz)	Max Freq (MHz)
H1, H2	1710	2690
M1, M2	1400	2025
L1 – L4	699	915

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6.2 2G Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
2G Transmitter Output						
Output Return Loss	S_{22}		-10		dB	50 load
Max Output Power, LB (GMSK)	P_{max}		3.8		dBm	
Max Output Power, HB (GMSK)	P_{max}		2.5		dBm	
Max Output Power, LB (8PSK)	P_{max}		5.5		dBm	
Max Output Power, HB (8PSK)	P_{max}		3.4		dBm	
Min Output Power (8PSK)	P_{min}		-66		dBm	
ORFS 400k, LB (GMSK)	$ORFS_{400k}$		-70		dBc	
ORFS 400k, HB (GMSK)	$ORFS_{400k}$		-67		dBc	
ORFS 400k, LB (8PSK)	$ORFS_{400k}$		-66		dBc	
ORFS 400k, HB (8PSK)	$ORFS_{400k}$		-65		dBc	
Modulation accuracy (GMSK)						
RMS phase error, LB	$_{RMS}$		0.4		deg	
RMS phase error, HB	$_{RMS}$		0.7		deg	
PEAK phase error, LB	$_{Peak}$		1.5		deg	
PEAK phase error, HB	$_{Peak}$		2.2		deg	
Modulation accuracy (8PSK)						
RMS EVM, LB	EVM_{RMS}		1.1		%	
RMS EVM, HB	EVM_{RMS}		1.9		%	
Peak EVM, LB	EVM_{Pk}		5.6		%	
Peak EVM, HB	EVM_{Pk}		8		%	
Origin offset suppression	OOS				dB	
Sideband suppression					dB	
Noise Emissions (GMSK)						
20MHz offset, LB			-167		dBc/Hz	at Pout=3.5dBm
32MHz offset, LB			-169		dBc/Hz	at Pout=3.5dBm
20MHz offset, HB			-162		dBc/Hz	at Pout=2.5dBm
32MHz offset, HB			-166		dBc/Hz	at Pout=2.5dBm
Noise Emissions (8PSK)						
20MHz offset, LB			-161		dBc/Hz	at Pout=-6dBm
32MHz offset, LB			-162		dBc/Hz	at Pout=-6dBm
68MHz offset, LB			-162		dBc/Hz	For G700 RX band noise
20MHz offset, HB			-157		dBc/Hz	at Pout = -3.2dBm
32MHz offset, HB			-158		dBc/Hz	at Pout = -3.2dBm

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6.3 3G FDD Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
3G FDD Transmitter Output						
Output Return Loss	S_{22}		-10		dB	50 load
Max Output Power (R99) Band 1 Band 2 Band 4 Band 5 Band 8	P_{max}		 5.2 5.4 5.4 7.6 7.5		 dBm dBm dBm dBm dBm	
Min Output Power (R99), all bands	P_{min}		-62		dBm	
Max Output Power (R6 16QAM) Band 1 Band 2 Band 4 Band 5 Band 8	P_{max}		 2.4 2.7 2.7 4.8 4.7		 dBm dBm dBm dBm dBm	
Min Output Power (R6 16QAM), all bands	P_{min}		-65		dBm	
RF Output Frequency Response	P		0.2		dB	±2.5MHz offset
ACLR1 (R99) Band 1 Band 2 Band 4 Band 5 Band 8			 -46 -46 -46 -48 -48		 dB dB dB dB dB	 at Pout=5dBm at Pout=5dBm at Pout=5dBm at Pout=5.5dBm at Pout=5.5dBm
ACLR2 (R99) Band 1 Band 2 Band 4 Band 5 Band 8			 -67 -68 -68 -71 -71		 dB dB dB dB dB	 at Pout=5dBm at Pout=5dBm at Pout=5dBm at Pout=5.5dBm at Pout=5.5dBm
RMS EVM (R99) Band 1 Band 2 Band 4 Band 5 Band 8			 2.3 2.2 2.2 2.1 2.1		 % % % % %	 at Pout=5dBm at Pout=5dBm at Pout=5dBm at Pout=5.5dBm at Pout=5.5dBm
Peak EVM (R99) Band 1 Band 2 Band 4 Band 5 Band 8			 8 8 8 6.6 6.6		 % % % % %	 at Pout=5dBm at Pout=5dBm at Pout=5dBm at Pout=5.5dBm at Pout=5.5dBm

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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ACLR1 (R6 16QAM) Band 1 Band 2 Band 4 Band 5 Band 8			 -45 -45 -45 -48 -48		 dB dB dB dB dB	 at Pout=2dBm at Pout=2dBm at Pout=2dBm at Pout=3dBm at Pout=3dBm
ACLR2 (R6 16QAM) Band 1 Band 2 Band 4 Band 5 Band 8			 -72 -72 -72 -72 -72		 dB dB dB dB dB	 at Pout=2dBm at Pout=2dBm at Pout=2dBm at Pout=3dBm at Pout=3dBm
RMS EVM (R6 16QAM) Band 1 Band 2 Band 4 Band 5 Band 8			 3.2 3.2 3.2 3 3		 % % % % %	 at Pout=2dBm at Pout=2dBm at Pout=2dBm at Pout=3dBm at Pout=3dBm
Peak EVM (R6 16QAM) Band 1 Band 2 Band 4 Band 5 Band 8			 12 12 12 12 12		 % % % % %	 at Pout=2dBm at Pout=2dBm at Pout=2dBm at Pout=3dBm at Pout=3dBm
Noise Emissions Band 1, noise in RX Band 2, noise in RX Band 5, noise in RX Band 8, noise in RX			 -163 -164 -163 -164		 dBc/Hz dBc/Hz dBc/Hz dBc/Hz	 at Pout=1.5dBm at Pout=1.5dBm at Pout=1dBm at Pout=1dBm

6.4 3G TDD Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
3G TDD Transmitter Output						
Output Return Loss	S_{22}		-10		dB	50 load
Max Output Power (QPSK)	P_{max}		5		dBm	
Min Output Power (QPSK)	P_{min}		-63		dBm	
Max Output Power (16QAM)	P_{max}		3		dBm	
Min Output Power (16QAM)	P_{min}		-65		dBm	
RF Output Frequency Response	P		0.2		dB	
ACLR1 (QPSK)			-47		dB	at Pout=3dBm
ACLR2 (QPSK)			-69		dB	at Pout=3dBm
RMS EVM (QPSK)			2		%	at Pout=3dBm

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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Peak EVM (QPSK)			5		%	at Pout=3dBm
ACLR1 (16QAM)			-47		dB	at Pout=1.5dBm
ACLR2 (16QAM)			-69		dB	at Pout=1.5dBm
RMS EVM (16QAM)			2		%	at Pout=1.5dBm
Peak EVM (16QAM)			7		%	at Pout=1.5dBm

6.5 LTE Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
4G FDD/TDD Transmitter Output						
Output Return Loss	S_{22}		-10		dB	50 load
Max Output Power Band 1 Band 7 Band 8 Band 13 Band 17 Band 21 Band 38 Band 40	P_{max}		 4 4.5 3.5 3 3 3.5 4 4		 dBm dBm dBm dBm dBm dBm dBm dBm	
Min Output Power, all bands	P_{min}		-65		dBm	
RF Output Freq. Response HB LB	P		 1 1.5		 dB dB	
EUTRA ACLR (Full RB) Band 1 Band 7 Band 8 Band 13 Band 17 Band 21 Band 38 Band 40			 -45 -43 -52 -55 -52 -45 -43 -45		 dB dB dB dB dB dB dB dB	 At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm
UTRA1 ACLR (Full RB) Band 1 Band 7 Band 8 Band 13 Band 17 Band 21 Band 38 Band 40			 -48 -46 -54 -57 -54 -47 -45 -47		 dB dB dB dB dB dB dB dB	 At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm At Pout = 0dBm

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Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
EUTRA ACLR (Partial RB)						
Band 1			-43		dB	At Pout = 0dBm
Band 7			-43		dB	At Pout = 0dBm
Band 8			-43		dB	At Pout = 0dBm
Band 13			-60		dB	At Pout = 0dBm
Band 17			-45		dB	At Pout = 0dBm
Band 21			-45		dB	At Pout = 0dBm
Band 38			-43		dB	At Pout = 0dBm
Band 40			-43		dB	At Pout = 0dBm
RMS EVM						
Band 1			1.5		%	At Pout = 0dBm
Band 7			1.8		%	At Pout = 0dBm
Band 8			0.9		%	At Pout = 0dBm
Band 13			0.9		%	At Pout = 0dBm
Band 17			0.8		%	At Pout = 0dBm
Band 21			1.4		%	At Pout = 0dBm
Band 38			2		%	At Pout = 0dBm
Band 40			1.8		%	At Pout = 0dBm
Peak EVM						
Band 1			**6**		%	At Pout = 0dBm
Band 7			**7**		%	At Pout = 0dBm
Band 8			**3**		%	At Pout = 0dBm
Band 13			**2**		%	At Pout = 0dBm
Band 17			**3**		%	At Pout = 0dBm
Band 21			**5**		%	At Pout = 0dBm
Band 38			**6**		%	At Pout = 0dBm
Band 40			**6**		%	At Pout = 0dBm
Noise in RX						
Band 1			-163		dBc/Hz	At Pmax
Band 7			-160		dBc/Hz	At Pmax
Band 8			-161		dBc/Hz	At Pmax
Band 13			-158		dBc/Hz	At Pmax
Band 17			-157		dBc/Hz	At Pmax
Band 21			-156		dBc/Hz	At Pmax

6.6 Transmitter Power Control Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Power detector						
RF Input Frequency	F_{det}	698		2690	MHz	
Input Return Loss	S_{11}		-10		dB	Ref. impedance 50
Maximum Input Signal	$P_{det,max}$			0	dBm	
Minimum Input Signal	$P_{det,min}$	-40			dBm	

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6.7 Harmonic Suppression

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
All Transmitter Outputs						
Harmonic Emissions						
2nd harmonic Band 1 Band 7 Band 8 Band 11 Band 13 Band 41			 -60 -50 -60 -60 -60 -55		 dBc dBc dBc dBc dBc dBc	
3rd harmonic Band 1 Band 7 Band 8 Band 11 Band 13 Band 41			 -25 -25 -20 -25 -55 -25		 dBc dBc dBc dBc dBc dBc	
4th harmonic Band 1 Band 7 Band 8 Band 11 Band 13 Band 41			 -40 TBD -40 -40 -60 TBD		 dBc dBc dBc dBc dBc	

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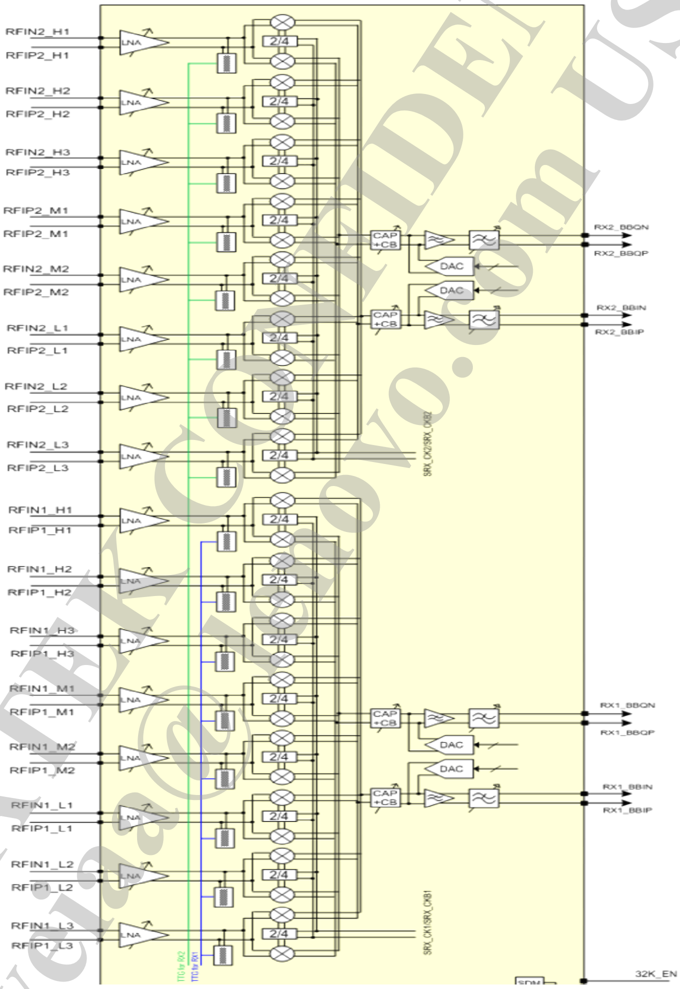
7 Receiver

The direct conversion/LIF receiver (RX) contains all active circuits for the complete receiver chain supporting LTE (TDD/FDD), single-cell (SC)/dual-cell (DC) 3G WCDMA, 3G TDSCDMA and 2G GSM/GPRS/EDGE (GGE) mode reception. IF frequencuy is 169.27kHz in 2G. The path contains a total of 8 LNAs (Low Noise Amplifier), 8 Mixers, 8 LO-Dividers, I/Q Current buffers, I/Q LPF1 and I/Q LPF2 analog filter.



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RX	Band supported
H3	1, 2, 3, 4, 7, 9, 10, 23, 25, 33, 38, 40, 41
H1, H2	1, 2, 3, 4, 7, 9, 10, 23, 25, 33, 34, 38, 39, 40, 41
M1, M2	1, 2, 3, 4, 9, 10, 11, 21, 24, 25, 33, 34, 39
L1, L2, L3	5, 6, 8, 12, 13, 14, 17, 18, 19, 20, 26, 27, 28

RX	Min Freq (MHz)	Max Freq (MHz)
H1, H2, H3	1805	2690
M1, M2	1475	2170
L1, L2, L3	734	960

B34,39 support at HB1/HB2/MB1/MB2

All LNAs have balanced inputs and are fully integrated. The quadrature LO signals are generated by a divider for all LNAs. The RF signal is down converted by high/low band quadrature direct-down-conversion mixers. The analog baseband filter is a low pass filter with programmable transfer function and gain controls. Besides, it contains an RC-calibration circuit, and a DC offset cancellation circuit (DCOC). Receiver power ON/OFF sequence, LNA/band selection, total receiver gain including LNA, mixer and analog baseband and DCOC timing are controlled by digital circuits. In addition, IQ calibration is done by injecting an offset frequency test tone generated by the test tone generator (TTG) into the RX mixer. Additional on-the-fly IQ imbalance tracking may be added in the DBB without changing the receiver design. The timing and control of this calibration scheme are also controlled by L1 software and digital circuitry. The spec. listed in 7.1~7.4 are guarantee when the IQ single end loading < 15pF.

7.1 2G Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Differential Input Impedance			100		Ω
Differential Input Return Loss	Note 1	-10			dB
Input Frequency	For all bands	869		1990	MHz
Noise Figure	Note 1; max gain; high band		2.5	3	dB
	Note 1; max gain; low band		2.5	3	dB
IIP3	±0.8MHz and ±1.6MHz offset	-12.5	-9.5		dBm
IIP2	±5.94MHz and ±6.06MHz offset	30	35		dBm

7.2 3G FDD Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Differential Input Impedance			100		Ω
Differential Input Return Loss	Note 1	-10			dB

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Parameter	Conditions	Min	Nom	Max	Unit
Input Frequency	For all bands	869		2170	MHz
Noise Figure	Note 1; max gain; high band		2.3	3	dB
	Note 1; max gain; low band		2.3	3	dB
IIP3	±10MHz and ±20MHz offset	-12.5	-9.5		dBm
	±3.5MHz and ±5.9MHz offset	-12	-9		dBm
	±3.5MHz and ±6.5MHz offset	-12	-9		dBm
	±3.5MHz and ±6.5MHz offset	7	10		dBm
	-80MHz (-38dBm) and -160MHz(-10dBm)	-7	-4		dBm
	-45MHz(-10dBm) and -90MHz(-38dBm)	-10	-7		dBm
IIP2	±4.5MHz and ±5.5MHz offset	50	55		dBm
	±14.5MHz and ±15.5MHz offset	30	35		dBm
IIP2 (TX offset)	All BWs, 44.9MHz, 45.1MHz offset (Band5, Band8)	48	53		dBm
	All BWs, 79.9MHz, 80.1MHz offset (Band2)	49	54		dBm
	All BWs, 189.9MHz, 190.1MHz offset (Band1)	50	55		dBm

7.3 3G TDD Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Differential Input Impedance			100		Ω
Differential Input Return Loss	Note 1	-10			dB
Input Frequency	For all bands	1880		2400	MHz
Noise Figure	Note 1; max gain.		2.3	3	dB
IIP3	±3.2MHz and ±6MHz offset	-12.5	-9.5		dBm
IIP2	±4.8MHz and ±4.9MHz	30	35		dBm

7.4 LTE Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Differential Input Impedance			100		Ω
Differential Input Return Loss	Note 1	-10			dB
Input Frequency	For all bands	728		2690	MHz
Noise Figure	Note 1; max gain; frequency < 2300MHz		2.3	3	dB

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Parameter	Conditions	Min	Nom	Max	Unit
	Note 1; max gain; frequency > 2300MHz		2.4	3.1	dB
IIP3 (WBIM)	BW=1.4MHz, ±6.3MHz and ±12MHz offset	-12.5	-9.5		dBm
	BW=3MHz, ±7.6MHz and ±7.8MHz offset				
	BW=5MHz, ±13.6MHz and ±13.8MHz offset				
	BW=10MHz, ±15.1MHz and ±15.3MHz offset				
	BW=15MHz, ±17.6MHz and ±17.8MHz offset				
	BW=20MHz, ±17.8MHz and ±35MHz offset				
IIP3 (TX+RX)/2, TX, Band 17	All BWs, 15MHz, 30MHz offset	-10	-7		dBm
IIP3 (ACS^3)	BW=1.4MHz, ±0.8MHz and ±1.3MHz offset				
	BW=3MHz, ±1.6MHz and ±2.6MHz offset				
	BW=5MHz, ±2.6MHz and ±4.6MHz offset				
	BW=10MHz, ±5.1MHz and ±9.6MHz offset	3	6		dBm
	BW=15MHz, ±7.6MHz and ±12.1MHz offset				
	BW=20MHz, ±10.1MHz and ±14.6MHz offset				
IIP2 (TX offset)	All BWs, 29.9MHz, 30.1MHz offset	48	53		dBm
	All BWs, 79.9MHz, 80.1MHz offset	49	54		dBm
	All BWs, 119.9MHz, 120.1MHz offset	50	55		dBm
IIP2 (IBB2 offset)	BW=1.4MHz, ±3.6MHz and ±3.8MHz offset	30	35		dBm
	BW=3MHz, ±7.6MHz and ±7.8MHz offset				
	BW=5MHz, ±13.6MHz and ±13.8MHz offset				
	BW=10MHz, ±15.1MHz and ±15.3MHz offset				
	BW=15MHz, ±17.6MHz and ±17.8MHz offset				
	BW=20MHz, ±20.6MHz and ±20.8MHz offset				

Note 1: Source/Reference impedance: 100 Ω

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8 Digital Control Interfaces

8.1 Introduction

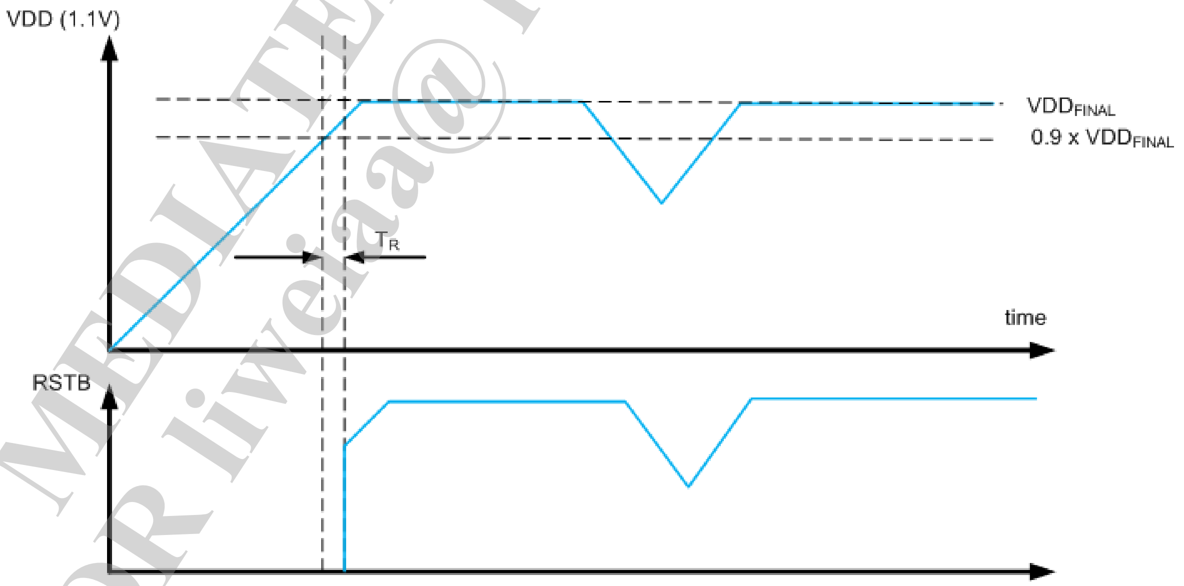
RFSYS is programmed through 5 BSI GPIO PADs. Both write and read operations are supported and 5 wires are used (3 bi-direction data pins, one clock pin, and one enable pin). All BSI interfaces are through VIO18 domain.

8.2 Power-on Reset

The chip includes two Power-On Reset (POR) operating from the static domain LDO's on the VXODIG domain. These operate on the DCXO_DIGITAL and GLOBAL_STATIC digital blocks from the 1.1V supply domain directly derived from VXODIG via LDO's. The designs are identical and since VXODIG is an "always-on" supply then a simplified implementation can be used - specifically there should not be situation where the VXODIG supply can drop after the internal LDO is enabled. The important point then is that the reset needs to be active for sufficiently long that the power supply has stabilized but short enough that the domain is available for BSI programming when requested.

In the case of the DCXO POR the LDO is directly enabled from the VXODIG supply. In the case of the GS LDO VXODIG is always present (in normal mode) and the LDO for this domain is enabled from the baseband.

The operation is shown in the figure below.



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Parameter	Conditions	Min	Nom	Max	Unit	Notes
Reset Active Time T_R	Over range of full VIO18 ramp times	5		200	µs	
VDD		0.8	1.1	1.25	V	
Trigger Point V_{TH}			0.9 x VDD		V	
Idd Quiescent current				<100	nA	

8.3 BSI Interface

The BSI Clock is designed to operate at a maximum frequency of 61.44 MHz, switching down to 30.72 MHz during the read back phase of a read operation.

The BSI clock has nominally a 50% duty cycle (< 40:60 should be guaranteed by the baseband clock generator). Following figure shows the timing diagram of write and read operations via BSI interface.

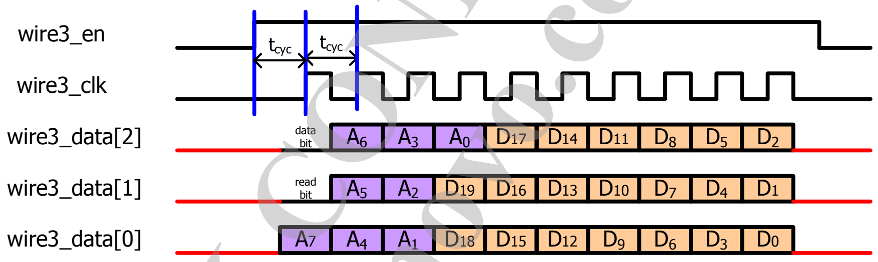

Figure 8-1. Timing diagram of write operation

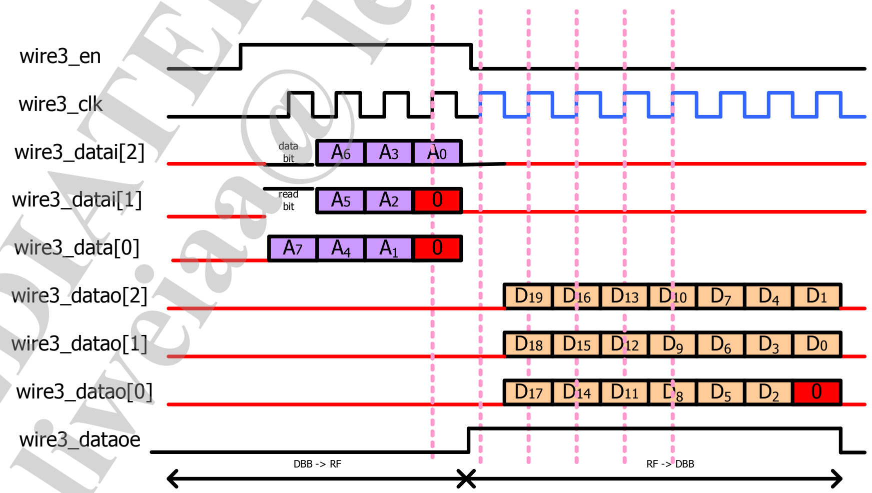

Figure 8-2. Timing diagram of read operation

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